



2

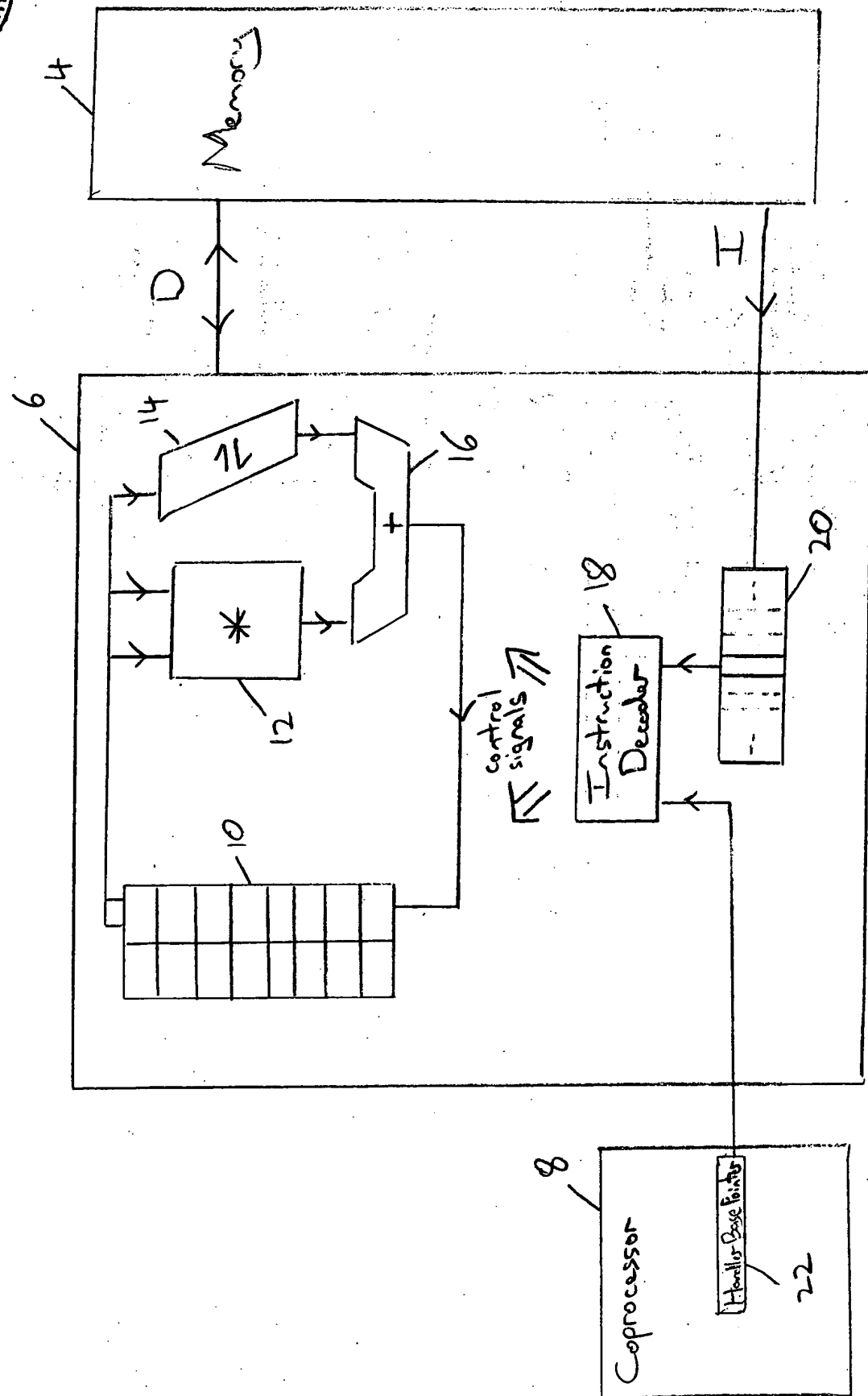
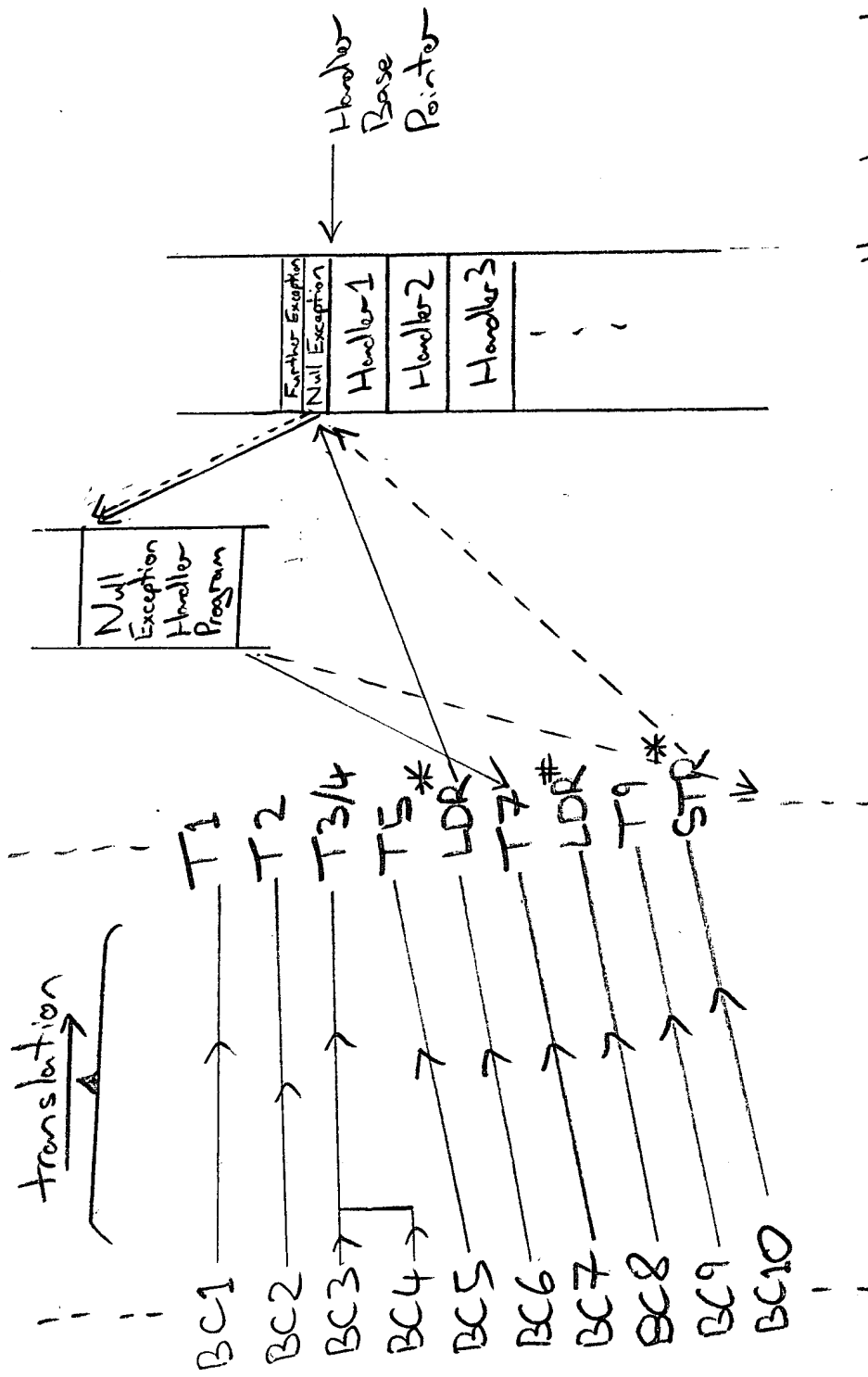


Fig. 1



Machine Independent Instructions

Thumb-2 Instruction

\* null value match

# null value non-match

Fig. 2

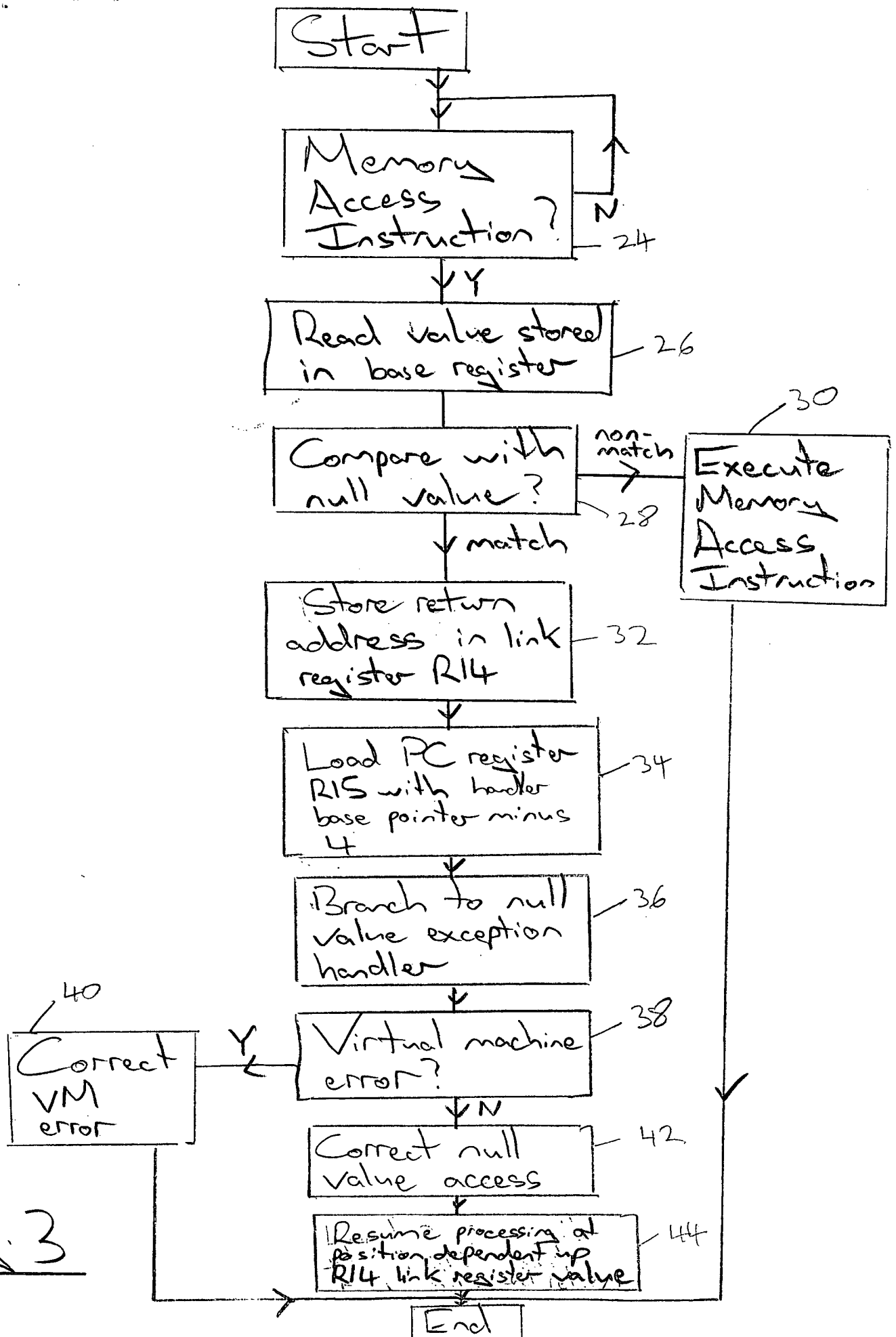


Fig. 3

Instruction	LDR.X Rd, [R9, #immediate.6]										
Encoding	15	14	13	12	11	10	9	8	3	2	0
	<LDR.X op code>							#immed_6		Rd	
Thumb-2 Equivalent	LDR Rd, [R9 <sup>‡</sup> + #immediate LSL #2]										
Definition	Rd = [R9 + #immediate LSL #2]										

Encoding space		2^8		8 bits							
<b>Note</b> This instruction, as are all loads and stores while in Jazelle-X state, is subject to the Null Check mechanism described in 4.3											
Instruction		STR.X Rd, [R9, #immediate.6]									
Encoding		15 14 13 12 11 10 9 8 3 2 0									
		STR.X opcode						#immed_6		Rd	
Thumb-2 Equivalent		STR Rd, [R9 + #immediate LSL #2]									
Definition		[R9 + #immediate LSL #2] = Rd									
Encoding space		2^8		8 bits							
<b>Note</b> This instruction, as are all loads and stores while in Jazelle-X state, is subject to the Null Check mechanism											

Fig 4

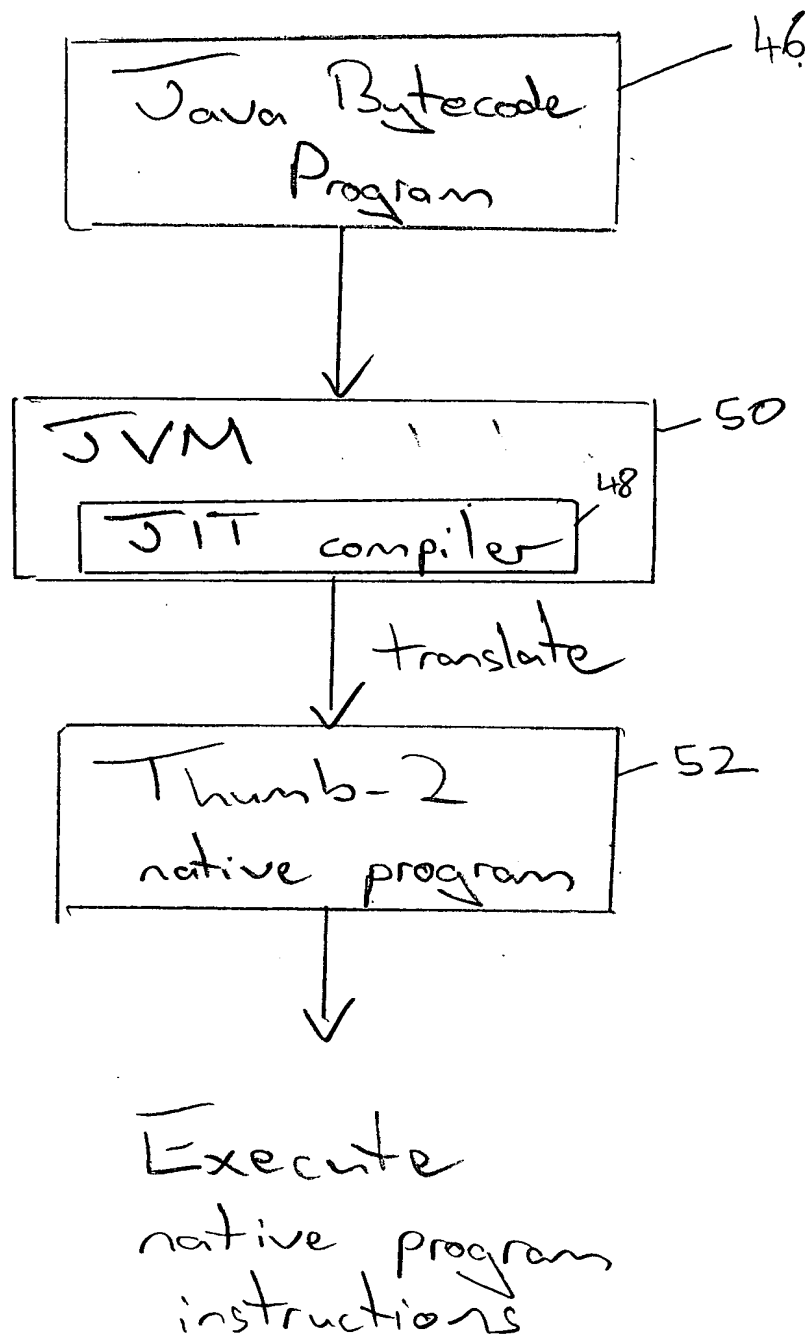


Fig. 5